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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,809	12/02/2003	Yue-Der Chih	TS00-749CIP	3324

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STEPHEN B. ACKERMAN
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

EXAMINER	
PHAN, TRONG Q	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,809	CHIH ET AL.	
	Examiner	Art Unit	
	TRONG PHAN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0504*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

It is not understood how the margin erase circuit in Fig. 5 of the present invention can be functioning properly as described in the lines 14-21, page 9 and lines 1-10, page 10 for the following reasons:

1) the terms m*Vt and n*V are not defined;

2) during the normal operation, how the voltage VE can be generated by the charge pump 36 and to be regulated into the normal erase voltage (VNE) since as shown in Fig. 5 of the present invention, the voltage VE is seen to be connected only to the gate of transistor 62, via diodes 46, in order to bias transistor 62 to be turned ON for conducting the output of charge pump circuitry 36 at the source of transistor 62 to the drain of transistor 62. How the output of the charge pump circuitry 36 can be pumped up to the voltage VE;

3) during testing, how the erase voltage VE, applied to the flash memory 58 through the high voltage switch 56, will be VME since VME is not shown in Fig. 5 of the present invention.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanbury, 6,236,597, in view of Kim, 6,249,455, and Del Signore et al., 6,002,355.

Sansbury, 6,236,597, discloses in Figs. 1-11 a system for developing high voltage (VEE)/normal erase voltage in the range of 10 volts to 16 volts (see lines 18-26, column 11), which is used to erase the flash memory cell, by charge pump circuits (see lines 18-44, column 11) and a reduced margin erase voltage during margin test procedure (see lines 13-42, column 15) in the range of –3 volts to 2 volts (see lines 47-48, column 15).

What is not shown in Sansbury, 6,236,597, is the charge pump circuit and the protective diode.

Kim, 6,249,455, discloses in Fig. 1 Prior Art a multi-step pulse generating circuit for providing a bias voltage OUT for erasing a flash memory device comprising:

positive charge pump 10;

a plurality of diode-connected transistors D11-D1n;

bias current source transistor N10;

bypass switches S11-S1n.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the multi-step pulse generating circuit in Fig. 1 Prior Art of Kim, 6,249,455, for modifying Sansbury, 6,236,597, for the purpose of having a uniform erase voltage according to the resistance of a diode chain (see lines 30-33, column 1 of Sansbury, 6,236,597).

What is not shown in Sansbury, 6,236,597, which is modified by Sansbury, 6,249,455, is the protective diode.

Del Signore et al., 6,002,355, discloses in Fig. 3 the teaching of using protective diode 37A' connected in reverse biased direction between power supply voltage VDD and the input of internal circuit 37A.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to modify in Sansbury, 6,236,597, which is modified by Sansbury, 6,249,455, by Del Signore et al., 6,002,355, for the purpose of preventing damage from electrostatic discharge (ESD) events (see lines 44-67, column 1 of Del Signore et al., 6,002,355).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tada et al., 5,297,101, Jungroth, 4,875,188, Javanifard et al., 5,455,794, Atsumi et al., 6,011,723, Itoh, 5,784,315, Yachareni et al., 6,370,061.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phan Trong

TRONG PHAN
PRIMARY EXAMINER